REMARKS

In response to the above-identified Office Action, Applicant seeks reconsideration in view of the following remarks. In this response, Applicant does not add, amend, or cancel any claims. Accordingly, claims 1-31 are pending.

I. Claims Rejected Under 35 U.S.C. § 103

Claims 1-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,651,163 issued to Kranich, et al. (hereinafter "Kranich") in view of U.S. Patent No. 6,425,039 issued to Yoshioka, et al. (hereinafter "Yoshioka"). Applicant respectfully disagrees for the following reasons.

To establish a *prima facie* case of obviousness, the Examiner must show the cited references, teach or suggest each of the elements of a claim. In regard to claims 1, 12 and 21, these claims include the elements of executing "a number of instructions at an address within a common interrupt handling vector address space ... wherein the number of instructions cause the processor to determine an identification of the processor based on a query that is internal to the processor." In the previous Office Action, Paper No. 7 of December 4, 2003, the Examiner relied on the thread control device and mapping table depicted in Figure 12 to teach these elements of the claims. The Examiner has changed his position in response to the Applicant's arguments in the Response mailed April 5, 2004 which pointed out that the thread control device and mapping table resided outside of the processor. The Examiner now cites col. 1, line 13-col. 2, line 33, the background and summary sections of Kranich, as teaching these elements. The Examiner also makes a vague statement that "Kranich teaches the well known concept of the use of a processor that processes queries related to both internal and external to the processor in order to help determine the identification of the processor." However, the Applicant has reviewed this cited section of Kranich and has been unable to discern any part therein that teaches these elements of claims 1, 12 and 21 or that even mentions a processor querying internal and external registers in order to determine the identification of the processor. Rather, the cited sections of Kranich discuss

the importance of hiding the multiprocessor nature of computer from an operating system to minimize overhead in the context of interrupt and exception handling. See col. 1, line 65 - col. 2, line 7 of Kranich. Thus, the Examiner has failed to set forth how the cited reference teaches or suggests each of the elements of the claim.

Further, the Examiner has failed to consider the claimed invention as a whole. See MPEP § 2141, Basic Considerations Which Apply to Obviousness Rejections. The Examiner argues that Kranich teaches a process that queries internal and external processors to determine the identity of the processor. However, the claims recite executing instructions within a common interrupt handling vector where these instructions cause the processor to determine identification of the processor with an internal query. The Examiner has not set forth any part of Kranich that teaches that an instruction from a common interrupt handler causes identification of the processor with an internal query. In fact, the Examiner admits that Kranich does not teach or suggest the concept of a common interrupt handling vector. See page 7, Paper No. 7. Thus, Kranich cannot teach an instruction within a common interrupt handler that causes an internal query to identify the processor. Therefore, the Examiner has failed to establish that Kranich teaches each of the elements of claims 1, 12 and 21.

The Examiner has not identified and Applicant has not been able to discern any part of Yoshioka that cures these defects of Kranich. Thus, the Examiner has not established that Yoshioka teaches or suggests each of the elements of claims 1, 12 and 21. Further, the Examiner improperly combined Yoshioka with Kranich. Kranich, as discussed previously, utilizes a thread control device and mapping table in a dynamic processor numbering scheme to coordinate the handling of interrupts and exceptions in a multiprocessor environment. Combining this system of Kranich with a common interrupt handling vector system of Yoshioka would change the principle of operation of Kranich. See MPEP § 2143.01, "The Proposed Modification Cannot Change The Principle of Operation of a Reference." Also, the Examiner has failed to provide a rational explanation as to how the cited references suggest the desirability of the proposed modification of

Kranich. See MPEP § 2143.01, "The Prior Art Must Suggest the Desirability of the Claimed Invention." Kranich teaches a system that is already capable of handling interrupts and exceptions in a multi-processor environment. The Examine has not provided any reference to any part of Kranich or Yoshioka that teaches the desirability of modifying Kranich to include a common interrupt handling vector. Thus, the Examiner has failed to establish a *prima facie* case of obviousness for independent claims 1, 12 and 21.

In regard to claims 2-6, 13-16 and 22-26, these claims depend from independent claims 1, 12 and 21 and incorporate the limitations thereof. Thus, at least for the reasons mentioned above in regard to claims 1, 12 and 21, these claims are not obvious over Kranich in view of Yoshioka. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

In regard to claims 8, 17 and 28, these claims include the elements of executing "a number of instructions at an address within the common interrupt handling address space of the same memory, wherein the number of instructions cause the processor to read a bit within an internal register to determine an identification of a processor in a multiprocessor system." In response to Applicant's previously submitted arguments that Kranich teaches the use of a thread control device and mapping table external to the processor, the Examiner again cites col. 1, lines 13 through col. 2, line 33 as teaching these elements of claims 8, 17 and 28. As discussed above in regard to independent claims 1, 12 and 21, this section of Kranich does not teach or suggest executing a set of instructions that are within a common interrupt handling vector where one of the instructions from within the common interrupt handling vector causes a processor to determine its identification based on a query that is internal to that processor including reading a bit within an internal register of that processor. The sections of Kranich cited by the Examiner makes no mention of reading bits in an internal register. Thus, the Examiner has failed to establish that Kranich teaches each of the elements of claims 8, 17 and 28 as set forth above in regard to independent claims 1, 12 and 21.

Yoshioka does cure these defects of Kranich and is not properly combined with Kranich. The Examiner has not indicated any part of Yoshioka that teaches these elements of claims 8, 17

and 28. The Examiner relies on the same rationale for combining Yoshioka with Kranich in relation to claims 8, 17 and 28 as is presented in regard to claims 1, 12 and 21. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for claims 8, 17 and 28. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

In regard to claims 9-11, 18-20 and 29-31, these claims depend from independent claims 8, 17 and 28, respectively, and incorporate the limitations thereof. Thus, at least for the reasons mentioned in regard to claims 8, 17 and 28, these claims are not obvious over Kranich in view of Yoshioka. Applicant again reminds the Examiner that the Examiner has not even set forth a basic argument or discussion of these claims and therefor has not set forth a *prima facie* case of obviousness for these claims. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

Claims 1, 8, 12, 17, 21 and 28 stand rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent Application No. 2002/00713154 by Brenner Jr., et al. (hereinafter "Brenner") in view of U.S. Patent No. 6,006,247 issued to Browning, et al. (hereinafter "Browning").

Claims 1, 12 and 21, include the elements of executing "a number of instructions at an address within a common interrupt handling vector address space ... wherein the number of instructions cause the processor to determine an identification of the processor based on a query that is internal to the processor." In the previous Office Action, Paper No. 7 of December 4, 2003, the Examiner admitted that Brenner did not teach or suggest these elements and relied on Browning, specifically the processor list in global memory depicted in Figure 2, to teach these elements of the claims. The Examiner has changed his position in response to the Applicant's arguments in the Response mailed April 5, 2004 which pointed out that the processor list in global memory resided outside of the processor, the Examiner now cites col. 1, line 20-col. 3, line 11, the background and summary sections of Browning as teaching these elements. The Examiner also makes a vague statement that "Browning teaches the well known concept of the use of a processor that processes queries related to both internal and external to the processor in order to

help determine the identification of the processor." However, the Applicant has reviewed this cited section of Browning and has been unable to discern any part therein that teaches these elements of claims 1, 12 and 21 or that even mentions a processor querying internal and external registers in order to determine the identification of a processor. Rather, the cited sections of Browning discuss the use of shared global memory and data structures including a global processor list and queue. See col. 2, line 46 - col. 3, line 11. Thus, the Examiner has failed to meet his burden to establish a *prima facie* case of obviousness as the Examiner has not set forth how the cited reference teaches each of the elements of the claim.

Further, the Examiner has failed to consider the claimed invention as a whole. See MPEP § 2141 entitled Basic Considerations Which Apply to Obviousness Rejections. The Examiner argues that Browning teaches a process that queries internal external processors to determine the identity of the processor. However, the claims recite executing instructions within a common interrupt handling vector where these instructions cause the processor to determine identification of the processor with an internal query. The Examiner has not set forth any part of Browning that teaches that an instruction from a common interrupt handler causes identification of the processor with an internal query. Thus, the Examiner has failed to establish that Kranich teaches each of the elements of claims 1, 12 and 21.

Further, the Examiner improperly combined Browning with Brenner. Brenner teaches a system for handling multiple interrupt types in different interrupt modes in a *uniprocessor* environment. Brenner, paragraphs [0005] - [0011]. Combining this uniprocessor system with a global memory and processor list structure of Browning would change the principle of operation of Brenner. See MPEP § 2143.01, entitled "The Proposed Modification Cannot Change the Principle of Operation of a Reference. Also, the Examiner has failed to provide a rational explanation as to how the cited references suggest the desirability of the proposed modification of Brenner. See MPEP § 2143.01, section entitled "The Prior Art Must Suggest the Desirability of the Claimed Invention." Brenner teaches a uniprocessor system that is capable of handling multiple interrupt

types. The Examiner has not provided any citation to either reference that teaches the desirability of modifying the multiple interrupt modes of Brenner for a multiprocessing environment. Thus, the Examiner has failed to establish a *prima facie* case of obviousness for independent claims 1, 12 and 21.

In regard to claims 8, 17 and 28, these claims include the elements of executing "the number of instructions at an address with a common interrupt handling address space of the same memory, wherein the number of instructions cause the processor to read a bit within an internal register to determine an identification of a processor in a multiprocessor system." The Examiner admitted in Paper No. 7 that Brenner did not teach these elements of the claims. In response to Applicant's previously submitted arguments that Browning teaches the use of a global memory and data structures external to the processor, the Examiner again cites col. 1, line 20 through col. 3, line 11 as teaching these elements of claims 8, 17 and 28. As discussed above in regard to independent claims 1, 12 and 21, this section of Browning does not teach or suggest executing a set of instructions that are within a common interrupt handling vector where one of the instructions from within the common interrupt handling vector causes a processor to determine its identification based on a query that is internal to that processor including reading a bit within an internal register of that processor. Thus, the Examiner has failed to establish that Brenner and Browning teach each of the elements of claims 8, 17 and 28. Further, as set forth above in regard to claims 1, 12 and 21, Brenner is improperly combined with Browning. The Examiner relies on the same rationale for combining Brenner with Browning in relation to claims 8, 17 and 28 as is presented in regard to claims 1, 12 and 21. Therefore, the Examiner has failed to establish a *prima facie* case of obviousness for claims 8, 17 and 28. Accordingly, reconsideration and withdrawal of the obviousness rejection of these claims are requested.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending, namely claims 1-31 patentably define the subject invention over the prior art of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207 3800.

Respectfully submitted,

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CERTIFICATE OF TRANSMISSION:

I hereby certify that this paper is being facsimile transmitted to the U.S. Patent and Trademark Office on September 14, 2004.

Lillian E. Rodriguez September 14, 2004 9-14-04